SV4E-I3C Exerciser

Complete Multi-lane I3C Protocol Exerciser

An **Introspect SV4E-I3C** is a 4-lane complete I3C protocol analyzer/exerciser that connects and autonomously operates as an I3C device thus enabling developers to completely verify their designs and characterize their performance margins. The highly integrated, portable, form factor and software environment allow for unprecedented ease of use when it comes to creating multiple I3C device roles on the bus.

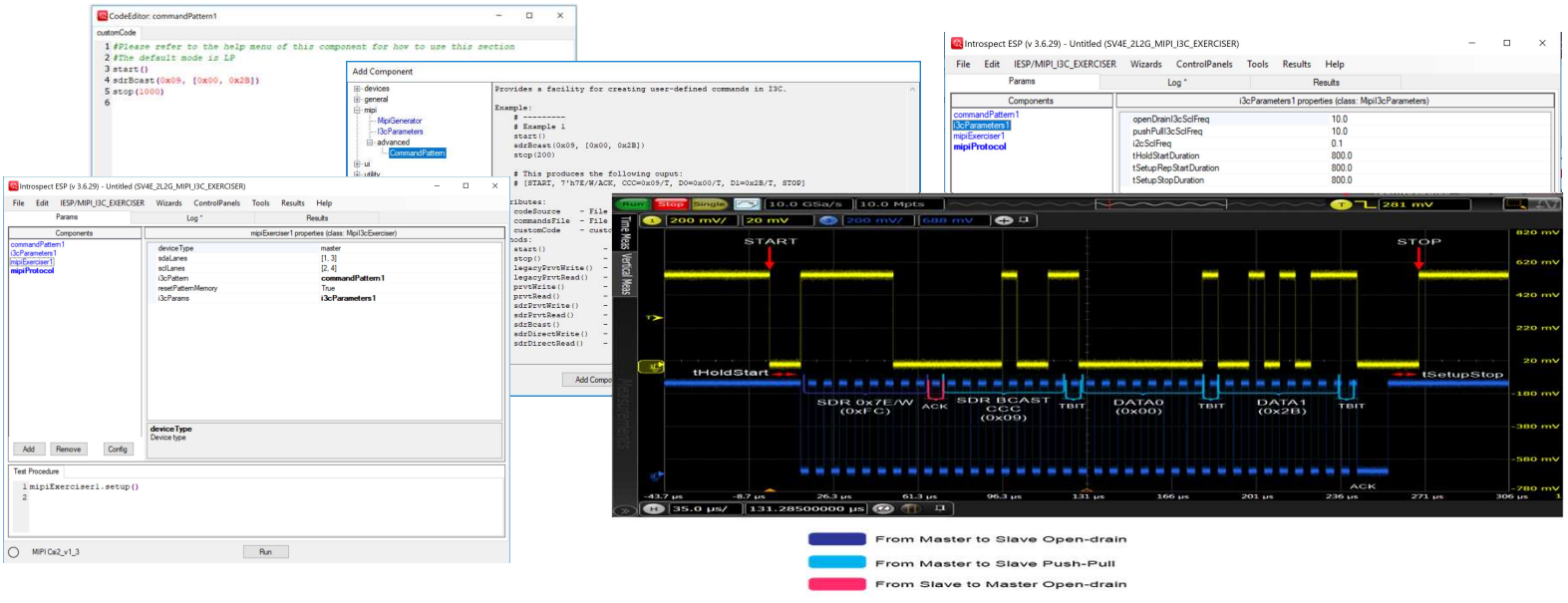
The **SV4E-I3C** allows high precision timing manipulation with a **5ns resolution** for the developer to ensure their designs work over a wide range of device interactions on the bus. It has deep vector memory thus it can be deployed as a MIPI Debug for I3C solution. The **SV4E-I3C** system has been designed around the MIPI I3C v1.x and I3C Basic 1.x specification standards.

Key Features

- **Device roles:** able to configure multiple devices from a single system onto the bus, such as main-master, secondary-masters, and I3C slaves
- **Lanes:** 4 lanes of SDA/SCL with each lane configured independently
- **Timing features:** high speed timing manipulation and control to 5ns for verifying setup and hold times including ACK responses
- **I3C protocol features:** easily generate CCC's and patterns for private and device-device communication, IBI, hot-join

Key Benefits

- **Self-contained:** bus controller with 4 lanes of MIPI I3C ports in an ultra compact form factor operating autonomously
- **Flexible:** solution featuring I3C and I3C Basic protocol support with real time voltage and timing controls
- **Automated:** scripting capability ideal for debug tasks, verification and full-fledged production screening of devices and system boards
- **Debug environment:** act as a bus slave to become a trace sink with complete readiness for MIPI Debug for I3C



Performance Characteristics

General Specifications

Feature	Description	Benefit
Bus Controller	I3C bus	Allows for multiple device role connection to the bus with SDR and HDR, in-band-interrupt, and hot-join support
Protocol	I3C + I3C Basic	Flexible software allows for closely tracking the rapid MIPI Alliance protocol evolution
Number Lanes	4	Tests high bandwidth sensors, IoT and high performance computing devices
Data Rate	Up to 33 Mbps	Provides a future-proof investment for next generation device data rates

Electrical Specifications

Feature	Description	Benefit
Voltage	1.2V	Optimized for low-voltage applications
Voltage Push/Pull	supported	Supports I3C devices
Voltage Open-drain	supported	Supports I2C legacy devices connected to an I3C and I3C
Per Wire Skew Injection Resolution	5 nS>	Enables executing characterization sweeps

Operating Modes

Feature	Description	Benefit
Device Roles	Main-Master Secondary Master I3C Slave Debug Test System interface	Able to connect to any Target System
Debug Pattern Memory	1 Gb	Provides deep vector memory for trace link debug
Multi-Port Features	Supported	Provides flexibility to operate in multiple user environments: hot join, IBI

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